BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

REMARKS

Claims 7, 9, 14, 15, 16 and 17 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicant regards as his invention. The applicant respectfully submits that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated **September 16, 2003**.

Claim Objections

Claims 16 and 17 are objected to because of minor informalities. Taking the Examiner's comments into consideration, claims 16 and 17 have been amended. Therefore, withdrawal of the rejection of claims 16 and 17 is respectfully requested.

Claim Rejections under 35 USC §112

Claims 7-17 are rejected under 35 USC §112, first paragraph, as failing to comply with the enablement requirement.

Specifically, the Examiner asserts that the specification fails to describe insulating regions "protruding" from the bottom of a pad part. As discussed on page 11, lines 2-4 of the specification and shown in figure 2A the "insulating regions (21a) are regularly (periodically) disposed at a pitch P in the second frame area (27c)" of pad (27). Therefore, claims 7, 9, and 14-17 are amended to indicate that the insulating regions are disposed on bottom of the pad part.

Further, the Examiner asserts that the specification and figures do not support the limitation

that the area ratio of the first frame area (L1/W1) is larger than the area ratio of the second frame area (L2/W1) as recited in claims 7, 14, 16 and 17.

The Examiner might be confusing the pad 27 with the pad 50 shown in Fig.1. The first pad of the claimed invention does not correspond to the pad 50 but corresponds to the pad 27, which is shown in Fig.2A. Fig.1 shows insulating regions having three layers 22, 23 and 24 between one conductive region and another conductive region of the pad 27. The method for forming the pad 27 is described at page 13, line 3 through page 14, line 15.

Further, the Examiner asserts that the specification and figures do not support the limitation that the area ratio of the first frame area (L1/W1) is larger than the area ratio of the second frame area (L2/W1) as recited in claims 7, 14, 16 and 17. The Examiner insists that the statement in claims 7, 14, 16 and 17 implies that the area ratio of the first frame area (L1/W1) is larger than the area ratio of the second frame area (L2/W1) in the last two lines on page 3 of the Office Action. However, the applicant is at a loss to understand why the statement implies the above structure.

"An area ratio of a recess in a near wiring area" means Sr/Sn, where Sr is a square measurement (size) of the recess and Sn is a square measurement (size) of the near wiring area (27b). In Fig.2A, there are no insulating regions (21 a) in the near wiring area (27b). The region where the insulating regions (21 a) are not disposed corresponds to the recess. In the embodiment shown in Fig.2A, Sr/Sn=100% because Sr=Sn. "An area ratio of a recess in a second frame area" means Sr/Ss, where Ss is a square measurement of the second frame area (27c). In Fig.2A, the insulating regions (21 a) are disposed in the second frame area (27c). In the embodiment shown in Fig.2A,

Sr/Ss>0 because Ss=Sr+(a square measurement of the insulating regions (21 a)). Therefore, Sr/Sn is larger than Sr/Ss as defined in claim 7.

It appears that the Examiner confuses "the area ratio of ***the recess*** in the second frame area" with "the area ratio of the second frame area".

Claims 16 and 17 are further rejected under 35 USC §112, first paragraph, as failing to comply with the written description requirement.

Taking the Examiner's comments into consideration claims 16 and 17 have been amended. Therefore, withdrawal of the rejection of Claims 16 and 17 under 35 USC §112, first paragraph, is respectfully requested.

Claim Rejections under 35 USC §102

Claims 7-17 are rejected under 35 USC §102(e) as being anticipated by Harada et al. (U.S. Patent No. 6,417,575 B2).

The present invention is a semiconductor device having a pad capable of suppressing excess current concentration. As illustrated in Fig. 2a, the pad includes a large number of insulating regions (21a) in which specific ratios of dimensions are followed. For example, W1 corresponds to the width of the wiring portion (25). The pad is divided into three portions. A first frame area (27a) having a width of L1. A second frame area (27c) has a width L2 and contains several insulating regions (21a). A central area (27d) is contained in the middle of the pad and may contain a via hole.

The width L1 of the first frame area (27 a) is equal to or wider than the distance between insulating regions (21a). As illustrated in Fig. 2A, the total width of pad (27) corresponds to 2 x W2 + n x W3 as discussed on page 11, line 22 of the specification, W1 correspond to the distance L1 and W3 corresponds to the distance P2. As discussed in the example provided on page 12, lines 4-11, W1 is larger than the distance L1 and the ratio L1/W1 is 30 percent or higher.

Harada et al. describes a semiconductor device and method of manufacturing the same which includes a pad electrode and main electrode layer. This device includes a first interlayer insulating film (7) a first intra-layer insulating film (11). Please note that the pad portion of this device is wider than the wiring portion.

Harada et al. does not describe the area ratio of the first frame area is larger than the area ratio of the second frame area as recited in claims 7 and 14. Further, Harada et al. does not describe a square measurement of the recess in a near wiring area is larger than a square measurement of the recess in the near wiring area divided by a total square measurement of the recess in the second frame area as recited in claims 16 and 17.

The Examiner states that a plurality of insulating regions (341) are formed in the pad area (lines 7-8, page 6 of the Office Action). However, it appears that the insulating region (341) surrounds the section (240). Namely, four insulating partitions (341) disposed at four corners are connected with each other through insulating regions. The conductive regions (340) are disposed apart from each other. This structure is shown more clearly in Fig.67A. Insulating partitions (321) correspond to insulating partitions (341). Metal layers (320) correspond to the conductive regions

(340). In Fig.77A, the section (240) can be called "pad", but the conductive regions (340) cannot be called "pad" because the conductive regions (340) are disposed apart from the section (240) and do not electrically connected to the section (240) in the layer in which the conductive regions (340) are disposed. Namely, the conductive regions (340) are disposed outside the pad.

The insulating region (341) is interposed between the section (240) and the region (340) (see column 32, lines 54-59). Namely, the insulating region (341) is disposed outside the section (240). Therefore, we cannot accept the Examiner's insistence that a plurality of insulating regions (341) are formed ***in*** the pad area.

Therefore, withdrawal of the rejection of Claims 7-17 under 35 USC §102(e) as being anticipated by Harada et al. (U.S. Patent No. 6,417,575 B2) is respectfully requested.

Conclusion

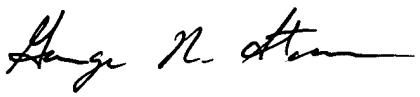
In view of the aforementioned amendments and accompanying remarks, claims 16 and 17, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, KRATZ, QUINTOS,
HANSON & BROOKS, LLP



George N. Stevens
Attorney for Applicant
Reg. No. 36,938

GNS/cmp
Atty. Docket No. **020029**
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

23850
PATENT TRADEMARK OFFICE

H:\HOME\GSTEVENS\02\020029\12-02-03 draft amendment